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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,743	01/21/2004	Kenichi Niiyama	12844.0065US01	3625

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EXAMINER	
BENENSON, BORIS	

ART UNIT	PAPER NUMBER
2836	

MAIL DATE	DELIVERY MODE
05/17/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/761,743	NIIYAMA ET AL.	
	Examiner	Art Unit	
	Boris Benenson	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 April 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/05/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Actions

1. Amendment received on 04/05/2007 is entered.

   a. Claim 1 is amended.

   b. Claim 6 is cancelled.

   c. Claims 1 and 3-5 are pending in the application.

   d. A set of formal drawings (4 sheets) received and approved.

Response to the arguments

2. Applicants argue that combination of Morikawa (5,091, 818) and Yoshimizu (5,451,814) does not teach limitations of Claim 1, which required "an external power terminal and a resistor electrically connected at one end to the external power terminal and at the other end to both the first voltage input terminal and the second voltage input terminal. Thus, the resistor and the voltage limiting means limit the input voltage applied to both the first and second voltage input terminals". Applicants argue that Morikawa "does not disclose a resistor connected at one end to both a first voltage input terminal and a second voltage input terminal" (as it noted in Office Action mailed on January 4, 2006). Applicants argue that Yoshimizu "does not

overcome these deficiencies". Examiner disagrees with such argument. Yoshimizu teaches a Multi-Chip Module Integrated Circuit comprising two IC chips (Fig. 2b, Pos. 21, 22), wherein each of the chips is connected to VCC power source through terminals: a first input terminal (31) and a second input terminal (35) are electrically connected. When teachings of Yoshimizu applied to a circuit disclosed by Morikawa the first voltage input terminal Morikawa (Fig.3, Pos. 13) and the second voltage input terminal Yoshimizu (Fig. 2b, Pos.35) are electrically connected and the resistor Morikawa (Fig.3, Pos. RD) is connected to both the first and second voltage input terminals at one end and to external power terminal (terminal of power source 11). The argument is not convincing. The rejection is maintained.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the

art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morikawa et al. (5,091,818) in view of Yoshimizu (5,451,814). Morikawa et al. disclose an Overvoltage Protection Circuit including an internal circuit (Fig.1, Pos. 31 or Fig.3, Pos. 15) with incorporated overvoltage protection. "For example, in a semiconductor integrated circuit used on a vehicle and receiving a power supply voltage from a vehicle battery, an overvoltage protecting circuit is incorporated for protecting an internal circuit upon an increase in battery voltage above a predetermined value by a surge or the like"(Col.1, Lines 13-18). The semiconductor integrated circuit comprises a voltage input terminal (Fig.1, Pos.33 or Fig.3, Pos.13), a voltage limiting means (Fig.1, pos.32 or Fig.3, Pos. 16) that limits applied voltage to a predetermined value, and an internal circuit read on circuit block (15) to which voltage, limited by the voltage limiting means is applied. An external power from a DC power source (Fig.1, Pos. 35 or Fig.3, Pos.11) is applied through a wiring (Fig.1, Pos.34 or Fig.3, Pos.12) to an external terminal of an external resistor (RD), connected between the voltage input terminal of the integrated circuit and the external terminal. A combination of a voltage drop on the

resistor and on voltage limiting means is limiting voltage Vcc to have the predetermine value when voltage applied to the external terminal becomes an overvoltage. Morikawa et al. did not disclose internal structure of the internal circuit and therefore did not disclose a second integrated circuit having a second voltage input terminal to which the input voltage is applied. Yoshimizu teaches a Multi-Chip Module Integrated Circuit, wherein two integrated circuit chips a first IC (Fig.2, Pos 21) and a second IC (Pos. 22) are connected to input voltage (VCC) by a bounding wire (Pos. 37). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Morikawa et al. with teachings of Yoshimizu and provide the same input voltage of the predetermine value to both the first and second integrated circuits, because it will protect entire circuitry.

Referring to Claim 3, Morikawa et al. disclose a voltage limiting means (Fig.1, Pos. 32) comprising a bipolar transistor (Pos. Q) connected between the voltage input terminal (33) and a ground (36) and at least one diode (Dz) connected in series between a base of the bipolar transistor and an input voltage point of the voltage limiting means.

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morikawa et al. (5.091.818) in view of

Yoshimizu (5,451,814) and Kawamoto (6,762,461). Morikawa et al. in view of Yoshimizu (5,451,814) disclose a circuit including all the limitation of Claim 1, as it was discussed above, but didn't disclose a Zener diode connected between the input voltage and a ground. Kawamoto teaches Semiconductor Element Protected With Plurality Of Zener Diodes. Figure 11, described as conventional protective circuit, indicates a Zener diode (Fig.11, Pos.D1) connected between input voltage terminal and the ground. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Morikawa et al. in view of Yoshimizu with teachings of Kawamoto and use a Zener diode connected between input voltage terminal and the ground as the voltage limiting means, because it will direct excessive voltage to the ground and therefore protect connected circuitry from overvoltage and because as teaches Kawamoto it is conventional.

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morikawa et al. (5.091.818) in view of Yoshimizu (5,451,814) and Chen U.S. Patent Application (10/272,061). Morikawa et al. in view of Yoshimizu disclose a circuit including all the limitation of Claim 1, as it was discussed above, but didn't disclose the voltage limiting means comprising a MOS transistor connected between voltage input

terminal and the ground, a first resistor connected between the gate of the MOS and input voltage, and a second resistor connected between the gate of the MOS and the ground. Chen teaches a High ESD Stress Sustaining ESD Protection Circuit, wherein a voltage on the gate of MOS is determined by voltage dividing ratio of a first resistor and a second resistor. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Morikawa et al. in view of Yoshimizu with teachings of Chen and use in a voltage limiting means a MOS transistor with a voltage divider connected to the gate of the MOS, because it will enable easily and reliably control a triggering point of the MOS and therefore provide stable supply of safe voltage to an integrated circuit.

THIS ACTION IS MADE FINAL.

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Boris Benenson whose telephone number is (571) 272-2048. The examiner can normally be reached on Mon -Fri (9-6).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Michael Sherry can be reached on (571) 272-2084. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system,

see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Boris Benenson
Examiner
Art Unit 2836

B.B.

5/12/07

MICHAEL SHERRY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800